REMARKS

Claims 1-36 are pending and are rejected. Reconsideration and allowance of Claims 1-36 are respectfully requested.

Amendments to Specification

Applicant amends paragraph [0093] to correct clerical errors. No new matter is introduced.

Claim Rejections under 35 USC §102 over Ohgane

Claims 1-3, 5-9, 12, and 16-36 are rejected under 35 USC §102(b) as being anticipated by Ohgane (USP 5,875,173). Applicant respectfully traverses these rejections.

Independent Claim 1

Applicant's Claim 1 recites:

A traffic management processor for processing an unspecified bit rate (UBR) traffic flow and a constant bit rate (CBR) traffic flow, comprising:

a departure time calculator (DTC) circuit for calculating a departure time for each packet received;

a content addressable memory (CAM) device coupled to the DTC circuit and having a plurality of rows, each row including a first portion for storing the departure time for a corresponding packet and including a second portion for storing a CBR bit indicating whether the corresponding packet belongs to the UBR traffic flow or to the CBR traffic flow; and

compare logic coupled to the CAM device and configured to determine which of the departure times stored in the CAM device is the earliest.

Ohgane fails to disclose or suggest a CAM in which each row includes a second portion *for storing **a CBR bit** indicating whether the corresponding packet belongs to the UBR traffic flow or to the CBR traffic flow*, as recited in Applicant's Claim 1.

The Office Action equates Ohgane's collating register 513 with the second portion of Applicant's CAM row that stores a CBR bit indicating whether the corresponding packet belongs to the UBR traffic flow or to the CBR traffic flow. However, in contrast to the Office Action's conclusion, Ohgane's collating register 513 does NOT store CBR bits indicating whether the corresponding packet belongs to the UBR traffic flow or to the CBR traffic flow, as recited in Applicant's Claim 1, ***but merely stores the match results*** for CAM array 511.

Indeed, Ohgane specifically states that a "collating register 513 having storage positions corresponding to the respective cell arrays is provided [in which] a logic level '1' is stored in a storage position corresponding to the matched cell array, while a logic '0' is stored in a storage position corresponding to the unmatched cell array.[1] Ohane further states that during compare operations in the CAM array 511, "if agreement between the counter value and the stored value is detected at step S9, a logical "1" representing "agreement" is stored in the collating register 513."[2] Thus, Ohgane's collating register 513 is a match result register that stores match results of the CAM array 511, NOT a CBR bit that indicates whether a corresponding packet is part of a CBR traffic flow or a UBR traffic flow.

The Office Action states that Ohgane "clearly discloses [the CAM device of Claim 1] since each row of it includes all the information of the row of application, including departure time and the bit that can be used to determine whether the packet belongs to a specific traffic type such as CBR," and notes that "some pieces of information may be located in other parts of the CAM device." However, the Office Action has NOT pointed to any language in Ohgane that discloses a CAM having CBR bits that indicate whether corresponding individual packets belong to a CBR traffic flow or a UBR traffic flow. Indeed, although Ohgane mentions that its control device can be configured to ***operate*** in either ABR mode or CBR mode, there is no language in Ohgane that discloses a ***CBR bit stored in a second portion of a CAM row*** that indicates which type of traffic flow the corresponding packet belongs to.

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1 Ohgane, col 8, lines 47-52 (emphasis added).
2 Ohgane at col. 10, lines 21-23.

To anticipate a claim under 35 USC §102, each and every element of the claim must be disclosed in a single reference[3]. The exclusion of a claimed element from a prior art reference is typically enough to negate anticipation under 35 USC §102. Thus, because Ohgane fails to disclose or suggest a traffic management processor including a CAM having a plurality of rows, each row including "a second portion for storing a CBR bit indicating whether the corresponding packet belongs to the UBR traffic flow or to the CBR traffic flow," as recited in Applicant's Claim 1, Claim 1 is patentable over Ohgane. Accordingly, Applicant respectfully requests the Office to withdraw the rejection of Claim 1.

Claims 2-15 depend from Claim 1 and therefore distinguish over the cited references for at least the same reasons as Claim 1.

Independent Claim 16

Applicant's Claim 16 recites:

A traffic management processor for processing a plurality of packets each having a control bit indicating whether the packet belongs to a traffic flow having an unspecified bit rate (UBR) or belongs to a traffic flow having a constant bit rate (CBR), comprising:

means for generating a departure time for each packet in response to the control bit contained within the packet;

means for queuing the CBR packets and the UBR packets together in the same queue according to their departure times; and

means for selecting the CBR packets and the UBR packets for transmission according to their departure times.

The Office Action has failed to identify any language in Ohgane that discloses or suggests "queuing the CBR packets and the UBR packets together in the same queue," as recited in Applicant's Claim 16. Further, the Office Action has neither addressed nor refuted Applicant's argument that Ohgane fails to disclose "queuing the CBR packets and the UBR packets together in the same queue."

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3 Corning Glass Works v. Sumitomo Electric, 9 USPQ2d 1962, 1965 (Fed. Cir. 1989).

As known in the art, traffic flows are typically aggregated according to traffic type, and different traffic types are processed using different mechanisms or configuration modes. For example, in describing CBR and ABR traffic, Ohgane discusses different operating modes, and states that "in the CBR mode, the ATM switches 13a-13c control the peak rates TP1-TP3 to be constant in VC1-VC3 during data transfer. On the other hand, in ABR mode, the peak rates TP1-TP3 of VC1-VC3 can be changed during data transfer under the control of the ATM switches 13a-13c."[4] However, there is no language in Ohgane that discloses or suggests a "means for queuing the CBR packets and the UBR packets together in the same queue," as recited in Applicant's Claim 16.

Further, Ohgane describes its control device only with respect to the ABR mode, and specifically states that "although explanation has been made to the case where the present invention is applied to the ABR mode, the present invention is also applicable to the CBR mode."[5] Therefore, Ohgane only discloses that its control device can operate in a CBR mode; there is no language in Ohgane that discloses or suggests queuing both ABR and CBR packets ***together in the same queue***, as recited in Applicant's Claim 16. Accordingly, Claim 16 is patentable over Ohgane.

Claims 16-21 depend from Claim 16 and therefore distinguish over the cited references for at least the same reasons as Claim 16.

Independent Claim 22

Applicant's Claim 22 recites:

A traffic management processor for simultaneously processing an unspecified bit rate (UBR) traffic flow and a constant bit rate (CBR) traffic flow, comprising:

a departure time calculator (DTC) circuit configured to calculate a departure time for each UBR packet and configured to calculate a departure time window for each CBR packet;

a queuing mechanism coupled to the DTC circuit and configured to queue the UBR packets and the CBR packets together; and

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4 Ohgane, col. 6, lines 20-27.

5 See Ohgane, col. 11, lines 31-34.

compare logic coupled to the queuing mechanism and configured to select the packets for departure.

As discussed above with respect to Claim 16, the Office Action has failed to identify any language in Ohgane that discloses or suggests "means for queuing the CBR packets and the UBR packets together in the same queue." Accordingly, Ohgane fails to disclose or suggest a traffic management processor that includes "a queuing mechanism coupled to the DTC circuit and configured to queue the UBR packets and the CBR packets ***together*** (emphasis added)," as recited in Applicant's Claim 22, and therefore Claim 22 is patentable over Ohgane.

Claims 23-27 depend from Claim 22 and therefore distinguish over the cited references for at least the same reasons as Claim 22.

Independent Claim 28

Applicant's Claim 28 recites:

A method of processing a first traffic flow having an unspecified bit rate (UBR) and a second traffic flow having a constant bit rate (CBR), comprising:

calculating a departure time for each packet received;

storing the departure times for packets belonging to all traffic flows in the same table, each departure time having a CBR bit;

asserting the CBR bit for each packet that belongs to the CBR traffic flow;

de-asserting the CBR bit for each packet that belongs to the UBR traffic flow;

determining which of the departure times that have a de-asserted CBR bit is the earliest; and

transmitting the packet corresponding to the earliest departure time.

First, as discussed above with respect to Claims 16 and 22, the Office Action has NOT identified any language in Ohgane that discloses "queuing the CBR packets and the UBR packets together," and similarly has not identified any language in Ohgane that discloses "storing the departure times for packets belonging to all traffic flows in the same table," as recited in Applicant's Claim 28.

Second, Ohgane does not disclose or suggest "asserting the CBR bit for each packet that belongs to the CBR traffic flow" and "de-asserting the CBR bit for each packet that belongs to the UBR traffic flow," as recited in Claim 28. The Office Action equates the assertion and de-assertion of Applicant's CBR bits with the Ohgane's collating register 513. However, as discussed above with respect to Claim 1, Ohgane's collating register 513 is a match result register that stores ***match results*** of Ohgane's CAM array 511; it does NOT store CBR bits that indicate whether corresponding individual packets belong to a CBR traffic flow or a UBR traffic flow. Further, the Office Action has not identified any language in Ohgane that discloses or teaches using the collating register 513 for storing CBR bits indicating the traffic type of a corresponding packet.

Accordingly, because Ohgane does not disclose or suggest "storing the departure times for packets belonging to all traffic flows in the same table, each departure time having a CBR bit," "asserting the CBR bit for each packet that belongs to the CBR traffic flow," and "de-asserting the CBR bit for each packet that belongs to the UBR traffic flow," as recited in Applicant's Claim 28, Claim 28 is patentable over Ohgane.

Claims 29-32 depend from Claim 28 and therefore distinguish over the cited references for at least the same reasons as Claim 28.

Independent Claim 33

Applicant's Claim 33 recites:

A method of scheduling packets of traffic flows having either an unspecified bit rate (UBR) or a constant bit rate (CBR), comprising:

calculating a departure time for each packet received;

storing the departure times for the UBR packets and for the CBR packets in a content addressable memory (CAM) device;

comparing the departure times for the UBR packets with each other to determine which departure time is the earliest; and

transmitting the packet corresponding to the earliest departure time.

Ohgane does not disclose or suggest "comparing the departure times for the UBR packets with each other to determine which departure time is the earliest," as recited in Applicant's Claim 33.

The Office Action equates Ohgane's logic 511-516 with the recitation of "comparing the departure times for the UBR packets with each other" in Claim 33. However, Ohgane teaches that the packet time values are compared with a *separate* ***counter value***, NOT ***with each other*** as recited in Claim 33. Indeed, Ohgane specifically states that "when [the packet departure] time value (T) matches with a value identified by the counter 50, an address where this time value (T) is stored can be determined as a virtual channel VC for the next cell to be transmitted."[6] This is in marked contrast to Claim 33, which compares the departure times ***with each other*** *to determine which departure time is the earliest.*

Applicants note that comparing the departure times with each other to determine which departure time is the earliest (as recited in Claim 33), rather than comparing the departure times to a current time value (as taught by Ohgane), may allow the traffic management processor of Claim 33 to achieve increased throughput. More specifically, Applicants' specification states that comparing the departure times with each other allows for the selection of a packet for departure in response to every compare operation, independent of any current time value, thereby optimizing packet transmission rates by allowing packets to be continually transmitted.[7] In contrast, prior art systems that "compare departure times with a current time value to select packets for departure may experience idle time during which no packets are transmitted if there is not a match between the current time value and any of the packet departure times."[8] Therefore, Ohgane fails to disclose or suggest a comparing the departure times with each other to determine which departure time is the earliest, as recited in Claim 33.

Accordingly, because Ohgane does not disclose or suggest "comparing the departure times for the UBR packets with each other to determine which departure time is the earliest," as recited in Applicant's Claim 33, Claim 33 is patentable over Ohgane.

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6 Ohgane, col. 8, lines 19-22.

7 Applicants' Specification, paragraph [0062].

Claim 34 depends from Claim 33 and therefore distinguishes over the cited references for at least the same reasons as Claim 33.

Independent Claim 35

Applicant's Claim 35 recites:

A method of scheduling packets of traffic flows having either an unspecified bit rate (UBR) or a constant bit rate (CBR), comprising:

calculating a departure time for each UBR packet;

calculating a departure time window for each CBR packet;

queuing the CBR packets and the UBR packets together in the same queuing mechanism; and

selecting the packets for departure according to which packet has the earliest departure time.

As discussed above with respect to Claim 16, Ohgane teaches that its control device can be configured to ***operate*** in ***either*** a CBR mode ***or*** in an ABR mode. The Office Action has not identified any language in Ohgane that discloses queuing the CBR packets and the UBR packets together in the same queuing mechanism. In contrast, Ohgane's description discloses queuing only ABR packets in the queuing mechanism 51, and suggests accommodating both CBR packets and ABR packets by ***operating*** in ***either*** a CBR mode ***or*** a UBR mode.[9] Thus, because Ohgane neither discloses nor suggests "queuing the CBR packets and the UBR packets together in the same queuing mechanism," as recited in Applicant's Claim 35, Claim 35 is patentable over Ohgane.

Claim 36 depends from Claim 35 and therefore distinguishes over the cited references for at least the same reasons as Claim 35.

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8 Applicants' Specification, paragraph [0063].

9 Ohgane, col. 6, lines 20-27.

Claim Rejections under 35 USC §103

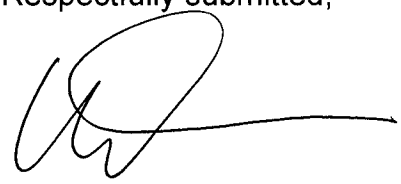
Claims 4, 10-11, and 13-15 are rejected under 35 USC §103(a) as being unpatentable over Ohgane. Applicant respectfully traverses these rejections.

Claims 4, 10-11, and 13-15 depend from Claim 1 and therefore distinguish over the cited references for at least the same reasons as Claim 1.

## CONCLUSION

In light of the above remarks, it is believed that Claims 1-36 are in condition for allowance and, therefore, a Notice of Allowance of 1-36 is respectfully requested. If the Examiner's next action is other than allowance as requested, the Examiner is requested to call the undersigned at (408) 236-6646.

Respectfully submitted,



8/6/2007
Dated

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